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(d) generating a plasma of said etching gas at a second power level in said chamber and contacting said integrated circuit substrate with said second power level plasma for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma, and wherein said substrate has a CD loss decreased compared to the CD loss of a substrate formed by a method comprising said steps (a), (b) and (c) but not step (d).

93. (New) The integrated circuit substrate of claim 92, wherein said CD loss is legreased by about 400 Angstroms.